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3 APPLICATION  
4 FOR  
5 UNITED STATES LETTERS PATENT  
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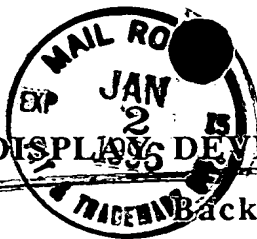
7 Be it known that I, Youichi Imamura, a citizen of Japan, of 3-5  
8 Owa 3-chome, Suwa-shi, Nagano-ken, 392 Japan, c/o Seiko Epson  
9 Corporation, have invented new and useful improvements in:

10 FLAT DISPLAY DEVICE AND DISPLAY BODY DRIVING DEVICE  
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12 of which the following is the specification:  
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## FLAT DISPLAY DEVICE AND DISPLAY BODY DRIVING DEVICE



## Background of the Invention

Technical Field:

The present invention relates generally to a flat display such as liquid crystal display (LCD) and plasma display panels and also applied devices thereof, and more particularly, to a flat display device having such a configuration that a display body module and a display control unit for controlling the display are separately disposed as well as to a display body driving device.

Background Art:

A portable personal computer and word processor known as a so-called laptop type generally have hitherto incorporated an opening/closing type flat display unit. Middle-and-large-sized liquid crystal display devices mounted therein each consist of, as illustrated in FIG. 9, a liquid crystal display unit 10 built into the device body and a flat liquid crystal display module unit 20 provided inwardly of an opening/closing cover so that these units are separately independently disposed. The liquid crystal display control unit 10 includes a liquid crystal module controller 12 and a microprocessor unit (MPU), not shown. The liquid crystal module controller 12 supplies a variety of control signals and clock signals to liquid crystal display module unit 20. The liquid crystal display module unit 20 has, e. g., a simple matrix type liquid crystal display panel (matrix liquid crystal display elements) 22; a signal electrode driving circuit (X drivers) 24 and a scan electrode driving circuit (Y drivers) 26 which are TAB-packaged in peripheral regions (frame) of the panel 22; and a liquid crystal power source circuit 28 for generating high

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liquid crystal driving voltages (reference voltages)  $V_0 - V_5$ . Signal electrode driving circuit 24 is composed of a plurality of signal electrode driver semiconductor integrated circuits  $24_1 - 24_m$  which are cascade-connected. Signal electrode driving circuit 24 supplies driver outputs per picture line to, e. g., M-pieces of signal electrodes in total. More specifically, data signals  $D_0 - D_7$  are sequentially taken in a shift register within the signal electrode driving circuit 24 by pixel clocks (shift clock pulses) XSCL. When the signals (M bits) per picture line are taken in, the data signals within the shift register are transmitted in parallel to a data latch circuit by scan line synchronous signals (data signal latch clocks LP) YSCL. The data signals undergo series/parallel conversion. The data latch circuit holds a signal voltage per line during a 1-scan period. Based on this signal voltage, a selection switch circuit sets output voltages of drivers connected to the signal electrodes either in a selection state or in a non-selection state. The AC-transforming clock FR is a clock for transforming each voltage described above into an AC waveform in order to prevent a deterioration of the liquid crystal elements due to a DC drive. A forced blank display signal DF is conceived as a signal for forcibly bringing a liquid crystal picture into a blank display state. The scan electrode driving circuit 26 consists of a plurality of scan electrode driver semiconductor integrated circuits  $26_1 - 26_n$  which are cascade-connected. The circuit 26 works to give a section voltage to only one of a total of N pieces of scan electrodes and non-selection voltages to the rest of them, i. e., (N - 1) pieces of scan electrodes. A 1-scan line period is started by the scan start pulse (frame start signal) SP. Every time a scan line synchronous

1 signal YSCL (data signal latch clock LP) comes, the selection voltages  
2 are sequentially impressed on the scan electrodes from the first line  
3 electrode to the N-th line electrode (line sequence display). The  
4 liquid crystal power source circuit 28 disposed on the side of the  
5 liquid crystal display module unit 20 generates a plurality of liquid  
6 crystal driving voltages  $V_0 - V_5$  selected by the selection switch of  
7 the scan electrode driving circuit 26 and the signal electrode driving  
8 circuit 24. The liquid crystal power source circuit 28 is set in power  
9 on/off states by the forced blank display signal DF.

10 The liquid crystal display control unit 10 built in the device body  
11 is connected to the flat liquid crystal display module unit 20  
12 typically through a hinge-connected movable part by using a flexible  
13 cable 30. With this arrangement, the cable 30 itself is bent every  
14 time the opening/closing cover on the side of the flat liquid crystal  
15 display module unit 20 is opened and closed. Signal lines of the  
16 cable 30 tend to be damaged or disconnected due to physical factors.  
17 If a part of the signal lines are disconnected, there arises a situation  
18 where no AC drive is effected in such a state that a DC voltage (DC  
19 component) remains impressed on, e. g., a liquid crystal display panel  
20 22. Deterioration of the liquid crystal display panel 22 is caused  
21 which is more expensive than other parts and therefore difficult to  
22 exchange. This liquid crystal deterioration is conceived as a factor of  
23 obstacle to display quality and life-span. This is a serious problem to  
24 the display device based on visual recognizability. Among the  
25 signals supplied to the liquid crystal display module unit 20 from the  
26 liquid crystal module controller 12, the signals which may induce a  
27 decline of the DC drive of the liquid crystal display panel 22 are a  
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1 scan start pulse SP, a scan line synchronous signal YSCL (data signal  
2 latch clock LP), an AC-transforming clock FR, and a logic-side power  
3 source voltage Vcc. When some operational abnormalities occur in  
4 the liquid crystal module controller 12 and the microprocessor unit  
5 (MPU), abnormalities arise in the respective signals. There exists a  
6 possibility where the situation similar to the above-mentioned may  
7 take place.

8 Expanding the problem about the DC drive of the liquid crystal  
9 display body, this can be generalized to a problem associated with a  
10 signal abnormality on the side of the liquid crystal module unit.  
11 Besides, where a wall-mounted TV is presumed, because of a display  
12 control unit and a display panel being disposed in remote places, a  
13 problem in terms of deterioration in display quality is produced due  
14 to attenuation of signal level and the influence of noise as well as  
15 signal stoppage. Furthermore, problems also occur not only in liquid  
16 crystal displays but also plasma displays.

17 Accordingly, it is an object of the present invention devised in  
18 light of the above-described problems to provide a flat display  
19 device and a display body driving device which are capable of  
20 preventing deterioration of display characteristics due to a DC drive  
21 of a display panel, this deterioration being derived from an  
22 abnormality of a signal supplied from a display control unit to a  
23 display body module unit.

#### 24 Disclosure of the Invention

25 Generally in a flat display device wherein a display body module  
26 unit and a display control unit for controlling the display thereof are  
27 separately disposed, the display body module unit performs passive  
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operations while following up control signals given from the display control unit. The present invention, however, adopts an autonomous signal system including a signal management control means. All of the components of the signal management control means can be provided on the side of the display body module unit. Those components may, however, be disposed distributively on the side of the display body module unit and in the display control unit.

Such a signal management control means consists of a signal detection means for detecting an occurrence of abnormality of a first signal transferred from the display control unit and a sequence processing means for changing a signal mode on the side of the display body module unit on the basis of the output thereof. The signal abnormality implies signal stoppage, a shrinkage in logic amplitude and an interference. A typical example may be the signal stopping. A liquid crystal display device and a plasma display device may be exemplified as a flat display device. The signal detection means is composed concretely of a signal stop detection means for detecting a stop of a first signal. The sequence processing means is a forced stop control means for control-setting, to zero, a display body application voltage supplied to a display panel body of a display body driving means on the basis of the output thereof. When the first signal is stopped on the side of the display body module, this stop is detected by the signal stop detection means. The display body driving means is thereby controlled by the forced stop control means. The driving means sets the display body application voltage to zero. Hence, even when stopping the first signal such as a clock or

the like, DC drive of the display body of the liquid crystal is avoided, thereby preventing deterioration of the display characteristics.

The following is an adoptable arrangement of the concrete forced stop control means. The forced stop control means includes a first signal delay means for delaying a second signal transferred from the display control unit by an output of the signal stop detection means. Display on/off of the display body driving means is controlled based on the output thereof. With such an arrangement, as a matter of course, the display on the liquid crystal panel can be quickly set in an off-state upon generating the detection signal. When the first signal resumes, however, the action is not that the display-on state is restarted at that moment but that the display body driving means is control-set in a display-on state after a time predetermined based on a cycle of the second signal has elapsed. Such a display body driving means control method, in terms of time difference, is capable of preventing an abnormal drive due to an abnormality of the power source, the abnormality being induced from a rush current. This control method is also capable of reducing a power source load and simplifying a power source circuit. The signal delay means receives a frame start signal as a second signal and is desirably N-staged D-type flip-flops settable and resettable, based on an output of the detection means. A delay time in such a case is determined on the unit of frame period. Another adoptable arrangement is that a plurality of signal management control means are disposed on the side of the liquid crystal module. In this case, it is possible to simultaneously detect plural kinds of signals. The forced stop control means is provided with a third signal control terminal for controlling

the output thereof, whereby the plurality of signal management control means can be cascade-connected. In such a case, when any detected signal is stopped, display-off with respect to the display body driving means is controllable.

In order to further prevent deterioration of the display body due to the abnormal drive attributed to the rush current, it is desirable that the display body module be provided with a power source control means for controlling power on/off of a display body power source means for generating display body driving voltages. This power source control means controls power on/off of the display body power source means, corresponding to an output of the detection means. By this control process, after confirming an appearance of the first signal on the side of the display body module unit, the display body power source means is powered on. The following is an adoptable construction of the concrete power source control means. The power source control means includes a second signal delay means for delaying the second signal transferred from the display control unit by the output of the detection means. Based on the output thereof, power on/off of the display body power source means is controlled. With this arrangement, the output of the first signal is confirmed, and, after the time predetermined based on the cycle of the second signal has passed, the display body driving means is energized. For this reason, the power source control means receives an input of a display on/off signal as a second signal.

Where the power source control means is M-staged ( $< N$ ) D-type flip-flops which are set/reset by an output of the detection means, after energizing the display body power source means, the display



body driving means is put into a display-on state. This also contributes a reduction in the rush current. However, M and N are positive integers.

The signal management control means relative to the above-described construction is provided on a glass substrate on the side of the display body module unit. The signal management control means can be incorporated into a circuit of the display body driving device which is packaged on the side of the display body module unit. Namely, a display body driving means incorporating a signal management control function can be actualized. The conventional display body driving means is configured in the form of drivers LSI. The forgoing display body driving means with the signal management control function can be constructed as a semiconductor integrated circuit. Y drivers LSI among the drivers LSI are smaller in the number of I/O wires than X drivers LSI. Taking this fact into consideration, it is advantageous that the Y drivers are employed as the drivers LSI with the signal management control function. Liquid crystal display devices are classified roughly into a simple matrix type and an active matrix type. Drivers LSI with the signal management control function are desirably scan drivers or gate drivers.

#### Brief Description of the Drawings

FIG. 1 is a block diagram illustrating a whole configuration of a liquid crystal display device in an embodiment 1 of this embodiment;

FIG. 2 is a circuit diagram showing constructions of respective scan drivers and connective relations between drivers in the same embodiment;

FIG. 3 is a circuit diagram illustrating scan electrode driving cells of the scan driver in the same embodiment;

FIG. 4 is a timing chart, showing relations between a variety of signals in a liquid crystal display body module unit, of assistance in explaining the operation of the same embodiment;

FIG. 5 is a block diagram depicting a whole configuration of the liquid crystal display device in an embodiment 2 of this invention;

FIG. 6 is a circuit diagram showing constructions of the signal management control units of the respective scan drivers and connective relations between the drivers in the same embodiment;

FIG. 7 is a circuit diagram illustrating construction of a liquid crystal power source circuit in the same embodiment;

FIG. 8 is a timing chart, showing relations of a variety of signals in the liquid crystal display body module unit, of assistance in explaining the operation of the same embodiment; and

FIG. 9 is a block diagram depicting one configuration of a conventional liquid crystal display device.

#### Best Mode for Carrying out the Invention

Embodiments of the present invention will hereinafter be described with reference to the accompanying drawings.

#### (Embodiment 1)

FIG. 1 is a block diagram illustrating a whole configuration of a liquid crystal display device in an embodiment 1 of this invention. Note that in FIG. 1, the same components as those of FIG. 9 are marked with the like reference symbols, and the description thereof will be omitted.

Signal management control units 47 are incorporated into scan driver semiconductor integrated circuits (LSI)  $46_1 - 46_n$  combined to constitute a scan electrode driving circuit (Y drivers) of a liquid crystal display module unit 40 in this embodiment. A signal management control unit  $47_1$  of the first scan driver semiconductor integrated circuit  $46_1$  detects stoppage of a scanning line synchronous signal YSCL (data signal latch clock LP) applied to a terminal CKB1. The signal management control unit  $47_2$  of the second scan driver semiconductor integrated circuit  $46_2$  detects stoppage of a scan start pulse (frame start signal) SP applied to a terminal CKB2. A signal management control unit  $47_n$  of the n-th (e.g., third) scan driver semiconductor integrated circuit  $46_n$  detects stoppage of an AC-transforming clock FR applied to a terminal CKBn. The respective signal management control units  $47_1 - 47_n$  have signal stop detection control terminals  $S_1 - S_n$  and signal stop detection terminals  $T_1 - T_n$ . A forced blank display signal DFF of a high level voltage is normally supplied from the control circuit 10 to the signal stop detection control terminal  $S_1$  of the signal management control unit  $47_1$  of the first scan driver semiconductor integrated circuit  $46_1$ . The signal stop detection terminal  $T_1$  is connected to the signal stop detection control terminal  $S_2$  of the signal management control unit  $47_2$  of the second scan driver semiconductor integrated circuit  $46_2$ . The signal stop detection terminal  $T_2$  of the signal management control unit  $47_2$  of the second scan driver semiconductor integrated circuit  $46_2$  is connected to a signal stop detection terminal (e. g., the signal stop detection control terminal  $S_n$  of the n-th signal management control unit  $47_n$ ) of the

1 next stage. The signal stop detection terminal  $T_n$  of the n-th signal  
2 management control unit  $47_n$  is connected to forced blank control  
3 terminals DF of the scan drivers  $46_1 - 46_n$  and the signal drivers  $24_1$   
4 -  $24_n$ .

5 The signal management control units  $47_1 - 47_n$  of the respective  
6 scan drivers are, as illustrated in FIG. 2, cascade-connected.  
7 Configurations of the signal management control units  $47_1 - 47_n$  are  
8 the same. A detected signal of the signal management control unit  
9  $47_1$  is a data signal latch clock LP applied to the terminal CKB<sub>1</sub>. A  
10 detected signal of the signal management control unit  $47_2$  is a scan  
11 start pulse (frame start signal) SP applied to the terminal CKB<sub>2</sub>. A  
12 detected signal of the signal management control unit  $47_n$  is an AC-  
13 transforming clock FR applied to the terminal CKB<sub>n</sub>.

14 Now, an emphasis is placed on the signal management control unit  
15  $47_1$ , and the construction thereof will be explained. The signal  
16 management control unit  $47_1$  includes a signal stop detection circuit  
17 48 serving as a signal detection means for detecting stoppage of the  
18 detected signal and a sequence processing circuit 51 consisting of a  
19 signal delay circuit 49 and a logic circuit 50.

20 The signal stop detection circuit 48 is composed of: a first N-type  
21 MOS transistor  $Tr_1$  switched by a latch clock LP conceived as a  
22 detected signal and constituting a transfer gate; an inverter  $INV_1$  for  
23 inverting a phase of the latch clock LP; a second N-type MOS  
24 transistor  $Tr_2$  switched by an antiphase signal of the latch clock LP  
25 and constituting a transfer gate; a first capacitor  $C_{11}$  for effecting a  
26 charge and discharge in accordance with opening/closing operations  
27 of the first N-type MOS transistor  $Tr_1$ ; a second capacitor  $C_{12}$  for  
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1 effecting the charge and discharge in accordance with the  
2 opening/closing operations of the second N-type MOS transistor  $Tr_2$ ;  
3 a discharge resistor  $R_1$  for discharging an electric charge of the  
4 capacitor  $C_{12}$ ; and an inverter  $INV_2$  for outputting a charge level  
5 judgment signal by comparing a charge voltage of the second  
6 capacitor  $C_{12}$  with a threshold value  $V_{TH}$ . The first N-type MOS  
7 transistor  $Tr_1$ , the inverter  $INV_1$  and the second N-type MOS  
8 transistor  $Tr_2$  are combined to constitute a series exclusive keying  
9 circuit. The first N-type MOS constitutes a selective charge switch for  
10 the first capacitor  $C_{11}$ . The second N-type MOST transistor  $Tr_2$   
11 constitutes a selective charge switch for distributively transferring a  
12 charge of the first capacitor  $C_{11}$  to a second capacitor  $C_{12}$ .

13 The signal delay circuit 49 consists of: a D-type flip-flop 49a, in  
14 which the frame start signal SP serves as a clock input CK, including a  
15 reset terminal R connected to an output of the inverter  $INV_2$  and an  
16 input terminal D earthed; and a D-type flip-flop 49b, in which the  
17 frame start signal SP serves as a clock input, including a reset  
18 terminal R connected to the output of the inverter  $INV_2$  and an input  
19 terminal D connected to an output Q of the flip-flop 49a. The logic  
20 circuit 50 is constructed of an AND circuit which receives two inputs  
21 of the forced blank signal DFF from the control circuit 10 and an  
22 output Q of a flip-flop 49b.

23 FIG. 3 is a circuit diagram illustrating a typical scan electrode  
24 driving circuit (logic unit) other than the signal management control  
25 unit 47<sub>1</sub> of the scan driver 46<sub>1</sub>. Formed in array in this logic unit  
26 are multi-bit scan electrode driving cells 46<sub>11</sub>, 46<sub>12</sub>,... for applying  
27 voltages in the order of lines corresponding to a multiplicity of scan  
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electrodes. Turning to FIG. 3, there are illustrated the scan electrode driving cells 46<sub>11</sub>, 46<sub>12</sub> of the first and second bits and peripheral circuits thereof.

Attention is herein paid on the scan electrode driving cell 46<sub>11</sub>, and its configuration will be explained. This scan electrode driving cell 46<sub>11</sub> consists of: a D-type flip-flop 46a, in a shift register, started by the frame start signal SP and transferring this frame start signal SP to the next stage every time a scan synchronous signal YSCL comes; a line unit forced blank display control circuit 46b for performing a logic arithmetic operation by adding, to its bit selection output Q, a forced blank display signal DF supplied from the terminal T<sub>n</sub> of the n-th scan driver 46n; a line unit voltage level shift circuit 46c for converting an output thereof into a high voltage system logic amplitude from a logic system power source voltage ( $V_{CC} = 5v$ ); a total line forced blank display control circuit 46d for performing a logic arithmetic operation by adding the forced blank display signal DF to the AC-transforming clock FR; an AC-transforming clock voltage level shift circuit 46e for converting the AC-transforming clock FR into a high voltage AC-transforming clock FR<sub>H</sub> having a high voltage system logic amplitude from the logic system power source voltage ( $V_{CC} = 5v$ ); a positive/opposite 2-phase clock generation circuit 46f for inverting the high voltage AC-transforming clock FR<sub>H</sub> thereof to an antiphase high voltage AC-transforming clock FR<sub>H</sub>; a selection control signal generation circuit 46g for generating four pieces of selection control signals C<sub>1</sub> - C<sub>4</sub> in chained combinations from a pair of the high voltage AC-transforming clock FR<sub>H</sub> and the antiphase high voltage AC-transforming clock FR<sub>H</sub> and a pair of outputs 0, 0 of

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the line unit voltage level shift circuit 46c; and a selection switch 46h for alternatively convey-supplying scan electrode driving voltages  $V_5$ ,  $V_1$ ,  $V_0$ ,  $V_4$  to the scan electrodes in response to respective selection control signals  $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$ . A forced blank display control circuit is herein composed of the line unit forced blank display control circuit 46b and the total line blank display control circuit 46d. Note that the symbol  $INV_3$  represents an inverter for matching logic with respect to the line unit forced blank display control circuit 46b of the forced blank display control signal DF.

Next, the operation of this embodiment will also be explained with reference to FIG. 4. When turning on a logic power source  $V_{CC}$  of the liquid crystal display device at a time  $t_0$ , a reset signal having a pulse width of several  $\mu s$  - several ms is supplied to a power-on reset terminal RS of a liquid crystal module controller 12 from an MPU (not illustrated) in the same manner with the prior art. The liquid crystal module controller 12 is thereby initialized. During this initialization, a variety of signals outputted from the liquid crystal module controller 12 are generally in a stopping status. During this period, the forced blank display signal DFF assumes a low voltage level (hereinafter referred to as an L level). Hence, a liquid crystal power source circuit 28 is in a power-off state, while the liquid crystal driving power source voltages  $V_0$  -  $V_5$  remain in a non-generated state. Therefore, during this initialization, no DC component is applied between the liquid crystal electrodes, and deterioration in liquid crystal elements is prevented.

If over this period, as illustrated in FIG. 4, the forced blank display signal DFF changes from the L level to a high voltage level

(hereinafter referred to as an H level) at a time  $t_1$ , the liquid crystal module controller 12 generates the frame start signal SP, the data signal latch clock LP, and the AC-transforming clock FR. Now, the operation of the signal management control unit 47<sub>1</sub> of the scan driver 46<sub>1</sub> will first be described. The frame start signal SP is supplied to an input terminal CKA<sub>1</sub> of the signal delay circuit 49. The data latch clock LP is supplied to a detection terminal CKB<sub>1</sub> of the signal stop detection circuit 48.

During an H-level period of the data signal latch clock LP, the transistor Tr<sub>1</sub> of the signal stop detection circuit 48 assumes an on-status, whereas the transistor Tr<sub>2</sub> assumes an off-status. Hence, the capacitor C<sub>11</sub> is charged with electricity for this period. During an L level period of the data signal latch clock LP, the transistor Tr<sub>2</sub> of the signal stop detection circuit 48 is in the on-status, whereas the transistor Tr<sub>1</sub> is in the off-status. Therefore, a part of the electric charge supplied to the capacitor C<sub>11</sub> is transferred to a capacitor C<sub>12</sub>. A charging voltage of the capacitor C<sub>12</sub> increases with a generation of repetitive pulses of the data signal latch clocks LP. An input voltage of the inverter INV<sub>2</sub> comes to the threshold value V<sub>TH</sub> or less. An output INV<sub>OUT</sub> of the inverter INV<sub>2</sub> assumes the H level at a time  $t_2$ . Before the time  $t_2$ , the output INV<sub>OUT</sub> of the inverter INV<sub>2</sub> assumes the L level. Therefore, the output Q of the D-type flip-flop 49a of the signal delay circuit 49 is at the L level. For this reason, an output T<sub>1</sub> of the logic circuit 50 assumes the L level. Even when the output INV<sub>OUT</sub> becomes the H level at that moment, the output Q does not assume the H level at the time  $t_2$ . During a 1-frame period ( $T_F$ ) and a 2-frame period ( $2T_F$ ) of the frame start



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1 signal SP, the output Q is kept at the L level due to delayed storage  
2 action of the input signals of the D-type flip-flops 49b, 49a. At a  
3 time  $t_3$ , the output  $T_1$  of the logic circuit 50 assumes the H level.

4 The frame start signal SP is supplied to the detection terminal  
5  $CKB_2$  of the signal stop detection circuit 48<sub>2</sub> of the signal  
6 management control unit 47<sub>2</sub> Supplied to an input terminal  $CKA_2$  of  
7 the signal delay circuit 49<sub>2</sub> is the frame start signal SP defined as a  
8 cascade input  $DI_2$  coming from a cascade output terminal D0 of the  
9 scan driver 46<sub>1</sub>. The output  $T_1$  of the logic circuit 50 of the scan  
10 driver 46<sub>1</sub> is cascade-connected to the logic circuit 50 of the scan  
11 driver 46<sub>2</sub>. A capacitor  $C_{21}$  of the signal stop detection circuit 48<sub>2</sub> is  
12 fed with electric energy by repetitive pulses of the frame start  
13 signals SP. Similarly, the AC-transforming signal FR is supplied to a  
14 detection terminal  $CKB_n$  of the signal stop detection circuit 48<sub>n</sub> of the  
15 signal management control unit 47<sub>n</sub> in the scan driver 46<sub>n</sub>. Supplied  
16 to an input terminal  $CKA_n$  of the signal delay circuit 49<sub>n</sub> is the frame  
17 start signal SP defined as a cascade input  $DI_n$  coming from the output  
18 terminal D0 of the scan driver 46<sub>2</sub>. The output  $T_2$  of the logic circuit  
19 50 of the scan driver 46<sub>2</sub> is cascade-connected to the logic circuit 50  
20 of the scan driver 46<sub>n</sub>. A capacitor  $C_{n2}$  of the signal stop detection  
21 circuit 48<sub>n</sub> is charged with electricity by the repetitive pulses of the  
22 AC-transforming signals FR. The different periods and duty ratios of  
23 the data signal latch clock LP conceived as a detected signal, the  
24 frame start signal SP and the AC-transforming signal FR. For making  
25 coincident the comparative judgment times  $t_3$  of the inverters  $INV_1$   
26 -  $INV_n$  in the respective scan drivers, it is desirable that values (time  
27 constants) of discharge resistances  $R_1 - R_n$  and of the capacitors  $C_{11}$   
28

-  $C_{n1}$ ,  $C_{12}$  -  $C_{n2}$  be mutually adjustable. For this purpose, in this embodiment, as illustrated in FIG. 1, the scan driver is provided with external connection terminals for the resistances and the externally attached capacitors.

As described above, during a period from the on-time  $t_0$  of the logic power source  $V_{CC}$  to the time  $t_3$  when the outputs  $T_1$  -  $T_n$  of the logic circuit assume the H level, the L level outputs  $T_n$  are supplied to the forced display blank control terminals DF of the signal drivers and the scan drivers. A liquid crystal display panel 22 is therefore in a blank display state. More specifically, when the forced display blank control signal DF is at the L level, only a transistor  $F_1$  of the selection switch 46h of the scan electrode driving cell 46 remains in an on-state under control of the forced blank display control circuits 46b, 46d depicted in FIG. 3. A voltage of  $V_5$  (0v) is impressed on the scan electrodes, while an inter liquid crystal electrode voltage (liquid crystal applying voltage) is 0v. A period from the time  $t_0$  to the time  $t_3$  corresponds to a liquid crystal drive inhibit period. At time  $t_1$ , the liquid crystal power source circuit 28 is powered on, whereby the liquid crystal voltages  $V_0$  -  $V_5$  are generated. Those voltages are supplied to the scan and signal drivers. At a power source actuation time, the shift registers in the scan and signal drivers are in an unsteady state. The liquid crystal display continues to be blank-controlled up to the time  $t_3$ , however, it is therefore possible to avoid abnormal driving of the liquid crystal panel.

Next, when the output  $T_n$  becomes the H level at the time  $t_3$ , H-level voltages are supplied to the forced display blank control

1 terminals DF of the scan and signal drivers. The liquid crystal  
2 display panel 22 is thereby AC-driven by normal operations of the  
3 scan and signal drivers. A display picture is depicted on the liquid  
4 crystal panel 22. The symbol B of FIG. 4 indicates a liquid crystal  
5 driving period. The liquid power source circuit 28 and the logic units  
6 of the scan and signal drivers are powered on at the time  $t_1$ . At  
7 time  $t_3$  later than that time, the liquid crystal display panel 22 is  
8 driven. Therefore, since the power-on of the power source does not  
9 take place simultaneously, an excessive power source rush current is  
10 restrained. It is because, in addition to delayed action of the signal  
11 stop detection circuit 48 itself, the delayed action of the signal delay  
12 circuit 49 having a delay time of 1 - 2 frame periods functions  
13 effectively.

14 Now, it is presumed that an output of the data signal latch clock  
15 LP transmitted from the liquid crystal module controller 12 is  
16 stopped at a time  $t_4$  in the liquid crystal driving period B. During  
17 outputting of the data signal latch clock LP, sufficient electric energy  
18 is supplied to the second capacitor  $C_{12}$  of the signal detection circuit  
19 48<sub>1</sub> of the scan driver 46<sub>1</sub>. When the clock thereof is stopped, no  
20 electric charge is transferred to the second capacitor  $C_{12}$  from the  
21 first capacitor  $C_{11}$ . Besides, the electric charge of the second  
22 capacitor  $C_{12}$  is quickly discharged at a predetermined time constant  
23 via the discharge resistance  $R_1$ . An input voltage of the inverter  
24 INV<sub>2</sub> is gradually boosted. If that input voltage exceeds the  
25 threshold value  $V_{TH}$ , the output voltage INV<sub>OUT</sub> thereof assumes the  
26 L level at a time  $t_5$ . With this logic variation, the signal delay circuit  
27 49<sub>1</sub> is reset, and the output Q thereof becomes the L level. Hence, in  
28

1 spite of the fact that the forced display blank control signal DF is at  
2 the L level, the output  $T_1$  of the logic circuit 50<sub>1</sub> assumes the L level  
3 at the time  $t_5$ . This  $T_1$  output is cascade-inputted to the logic circuit  
4 50<sub>2</sub> of the scan driver 46<sub>2</sub>. Even when the frame start signal SP is  
5 being outputted, and output  $T_2$  of the logic circuit 50<sub>2</sub> becomes the L  
6 level. Further, the  $T_2$  output is cascade-inputted to the logic circuit  
7 50<sub>n</sub> of the scan driver 46<sub>n</sub>. Therefore, the output  $T_n$  of the logic  
8 circuit 50<sub>n</sub> assumes the L level even when the AC-transforming  
9 signal FR is being outputted. The output  $T_n$  thereof corresponds to  
10 the forced display blank control signal DF on the side of the liquid  
11 crystal display module unit 46. The liquid crystal panel 22 is  
12 thereby brought into a blank display state by using the forced  
13 display blank circuits 46b, 46d. Namely, only a transistor F<sub>1</sub> of the  
14 selection switch 46h of the scan electrode driving cell 46 shown in  
15 FIG. 3 is in the on-state. A voltage V<sub>5</sub> (0v) is fed to the scan  
16 electrodes, and the inter liquid crystal electrode voltage is thereby  
17 kept at 0v. For this reason, even if the data signal latch clock LP is  
18 stopped due to some cause, the liquid crystal elements are not driven  
19 by the DC components, thereby preventing deterioration of the liquid  
20 crystal beforehand. If the frame start signal SP or the AC-  
21 transforming signal FR is stopped due to some cause, the output  $T_n$   
22 becomes the L level. Similarly, the deterioration of the liquid crystal  
23 is prevented beforehand. Incidentally, during this liquid crystal  
24 drive inhibit period A, so far as the frame start signal SP and the AC-  
25 transforming signal FR continue, the second capacitor C<sub>22</sub> and the  
26 capacitor C<sub>n1</sub> are in a charged state; and the outputs of the inverters  
27 INV<sub>2</sub>, INV<sub>n</sub> assume the H level.  
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When the data signal latch clock LP begins to reappear at a time  $t_6$ , as described above, the second capacitor  $C_{12}$  is charged with electricity. The output  $INV_{OUT}$  of the inverter  $INV_1$  then becomes the H level. After 1 - 2 frame periods from the time when the output  $INV_{OUT}$  has become the H level, the output Q of the signal delay circuit 49<sub>1</sub> functioning as a timer assumes the H level at a time  $t_7$ . The output  $T_1$  of the logic circuit 50<sub>1</sub> thereby becomes the H level, and correspondingly the outputs  $T_2, T_n$  of the logic circuits 50<sub>2</sub>, 50<sub>n</sub> become the H level. Hence, the forced blank control signal DF on the part of the liquid crystal module unit 22 is changed to the H level, whereby the liquid crystal display panel 22 enters the liquid crystal driving period B.

Finally, when the forced display blank control signal DFF on the part of the liquid crystal display controller 12 assumes the L level at a time  $t_8$ , the output  $T_1$  of the logic circuit 50<sub>1</sub> is changed to the L level. The outputs  $T_2, T_n$  of the logic circuits 50<sub>2</sub>, 50<sub>n</sub> thereby become the L level. Therefore, the forced display blank control signal DF on the side of the liquid crystal display module unit 20 becomes the L level. The liquid crystal display panel 22 enters a display-off period C.

(Embodiment 2)

FIG. 5 is a block diagram illustrating the liquid crystal display device in an embodiment 2 of this invention. Note that in FIG. 5, the same components as those of FIG. 1 are marked with like reference symbols, and the description thereof will be omitted.

A scan electrode driving circuit (X drivers) of a liquid crystal display module unit 70 is composed of a plurality of scan drivers 76<sub>1</sub>

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- 76<sub>n</sub>. These scan drivers include signal management control units 77<sub>1</sub> - 77<sub>n</sub> identical with the signal management control units of the embodiment 1. Added to the respective signal management control unit 77<sub>1</sub> - 77<sub>n</sub>, as illustrated in FIG. 6, are power source power on/off control circuits 78<sub>1</sub> - 78<sub>n</sub> for controlling power on/off times of the liquid crystal power source circuit 28 for generating the liquid crystal driving voltages V<sub>0</sub> - V<sub>5</sub>. Each of the power source power on/off control circuits 78<sub>1</sub> - 78<sub>n</sub> is constructed of: an inverter INV<sub>3</sub> for inverting signals coming in input terminals S<sub>1</sub> - S<sub>n</sub> of the logic circuit 50<sub>n</sub>; 2-stage-connected D-type flip-flops 78a, 78b; and a logic circuit 78c for taking logic with respect to the signals coming from terminals P<sub>1</sub> - P<sub>n</sub> and the output Q. A signal delay circuit 79 of each signal management control unit 77 is constructed in such a way that a D-type flip-flop 79c of the third stage is additionally connected to the 2-stage-connected D-type flip-flops 49a, 49b of the signal delay circuit 49 in the embodiment 1. A power on/off signal of the power source voltage V<sub>CC</sub> on the logic side is supplied to an input terminal P<sub>1</sub> of a logic circuit 78c of the first scan driver 76<sub>1</sub>. An output PF<sub>1</sub> of the power source power on/off control circuit 78<sub>1</sub> in the first scan driver 76<sub>1</sub> is cascade-supplied to a terminal P<sub>2</sub> of the second scan driver 76<sub>2</sub>. An output PF<sub>2</sub> of the power source power on/off control circuit 78<sub>2</sub> in the second scan driver 76<sub>2</sub> of the previous stage, is cascade-supplied to a terminal P<sub>n</sub> of the n-th scan driver 76<sub>n</sub>. An output PF<sub>n</sub> of the power source power on/off control circuit 78<sub>n</sub> of the n-th scan driver 76<sub>n</sub> is supplied to a power-off terminal POFF of the liquid crystal power source circuit 28.

1 The liquid crystal power source circuit 28 is structured in the  
2 same way with the conventional example. This circuit, as depicted in  
3 FIG. 7, includes: a voltage transforming circuit 28a for generating a  
4 high voltage (20 - 40v) which is boosted based on the  $V_{CC}$  (5v)  
5 power source voltage; an npn-type transistor 28b for effecting on/off  
6 control depending on a value of the voltage supplied to the power-off  
7 terminal POFF; a pnp-type transistor 28c of a power switch for  
8 performing on/off operations interlocking with on/off operations of  
9 the transistor 28b; a smoothing capacitor 28d interposed between a  
10 collector thereof and the earth; and a voltage dividing circuit 28e for  
11 outputting the liquid crystal driving voltages  $V_0 - V_5$  from the  
12 charge voltage thereof.

13 The operation of the foregoing embodiment will next be explained  
14 with reference to FIG. 8. A power switch SW is closed at a time  $t_0$ .  
15 The logic power source  $V_{CC}$  of the liquid crystal display device is  
16 turned on. In the same manner as embodiment 1, a reset signal  
17 having a pulse width of several  $\mu s$  - several ms is supplied from an  
18 MPU to a power-on reset terminal RS of the liquid crystal module  
19 controller 12. The liquid crystal module controller 12 is thereby  
20 initialized. Hence, an output signal from the liquid crystal module  
21 controller 12 is generally in a stopping status. During such a period,  
22 the logic power source voltage  $V_{CC}$  is supplied to one input of the  
23 logic circuit 78c defined as an AND circuit of the first scan driver  
24 76<sub>1</sub>. The data signal latch clock LP does not yet, however, come out,  
25 and hence its output PF<sub>1</sub> assumes the L level. As a result, an output  
26 PF<sub>2</sub> of the second scan driver 76<sub>2</sub> is also at the L level. Besides, an  
27 output PE<sub>n</sub> of the n-th scan driver 76<sub>n</sub> also becomes the L level,  
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whereby a power-off terminal POFF of the liquid crystal power source circuit 28 is kept at the L level. For this reason, a base potential of the transistor 28b shown in FIG. 7 assumes an L level (0v), so that a boosted voltage is not supplied to the smoothing capacitor 28d. Therefore, the liquid crystal driving voltages  $V_0 - V_5$  are not generated. As is similar to embodiment 1, no DC component is applied between the liquid crystal electrodes during this initializing period. Deterioration of the liquid crystal elements is prevented.

Next, as illustrated in FIG. 8, a variety of signals are generated from the liquid crystal module controller 12 at a time  $t_1$ . The forced blank display signal DFF is changed from the L level to the H level. The frame start signal SP, the data signal latch clock LP, and the AC-transforming clock FR are generated. As explained in embodiment 1, upon the data signal latch clock LP starting to appear, the output INVOUT of the inverter INV<sub>2</sub> assumes the H level at a time  $t_2$ . For this reason, the output Q of the power on/off control circuit 78b becomes the H level at a time  $t_3$  which is later by a 1 - 2 frame period than the time  $t_2$ . The output PF<sub>1</sub> of the logic circuit 78c, therefore, becomes the H level. The outputs PF<sub>2</sub>, PF<sub>n</sub> of the logic circuits 78c of the second and n-th scan drivers 76<sub>2</sub>, 76<sub>n</sub> become the H level, correspondingly. The power-off terminal POFF of the liquid crystal power source circuit 28 is energized at the H level. In consequence of this, the transistor 28b is put into an on-state. The transistor 28c is also brought into the on-state because of a drop in voltage of an inter base/emitter resistance of the transistor 28c. The smoothing capacitor 28d is charged with electricity, thereby



generating the liquid crystal driving voltages  $V_0 - V_5$ . During a period from the time  $t_3$  to a time  $t_4$  when the next frame start signal SP arrives, the output Q of the D-type flip-flop 79c remains at the L level. The stage number of the D-type flip-flops of the signal delay circuit 79<sub>1</sub> in this embodiment is greater by 1 than in the power on/off control circuit 78<sub>1</sub>. The output Q of the D-type flip-flop 79c becomes the H level, but slower by a 1-frame period  $T_F$  than that of the D-type flip-flop 78b. As a result, the outputs  $T_{11}$ ,  $T_{27}$ ,  $T_n$  all become the H level. In the same manner as embodiment 1, the forced blank display signal DF on the part of the liquid crystal module unit is changed from the L level to the H level. The driving voltages  $V_0 - V_5$  are thereby supplied to the scan and signal electrodes of the liquid crystal display panel 22. The operation then enters a liquid crystal mode.

For instance, concurrently with generation of the liquid crystal driving voltages  $V_0 - V_5$ , the liquid crystal display panel 22 is driven. It follows that large charge rush currents are induced in power source units of the scan and signal drivers as well as in the liquid crystal panel. In accordance with this embodiment, however, the liquid crystal drive is initiated after the 1-frame period  $T_F$  since the liquid crystal driving voltages  $V_0 - V_5$  have been generated at the time  $t_3$ . The power source units are energized with a time difference, whereby the rush currents can be dispersed. This makes it possible to prevent a power-down and reduce power capacity, which is in turn helpful for protecting the liquid crystal display panel and the drivers as well. The above-described power control decreases burden in terms of system development costs and

1 restrains an increase in the number of signal wires between the  
2 conventional system and LCD module. Furthermore, a reduction in  
3 power capacity is brought about, and hence inexpensive power  
4 source is available.

5 Next, supposing that oscillations of the data signal latch clocks LP  
6 transmitted from the liquid crystal module controller 12 are stopped  
7 at the time  $t_5$  in the liquid crystal driving period B, as in  
8 embodiment 1, the input voltage of the inverter  $INV_2$  is boosted.  
9 The output voltage  $INV_{OUT}$  becomes the L level at a time  $t_6$ . The  
10 outputs  $T_1, T_2, T_n$  also become the L level. As a result, the forced  
11 display blank control signal DF on the side of the liquid crystal  
12 display module unit assumes the L level. The liquid crystal display  
13 panel 22 is thereby put into a blank display state. The effects as  
14 those of embodiment 1 are exhibited. When the output voltage  
15  $INV_{OUT}$  of the inverter  $INV_2$  assumes the L level, the outputs  $PF_1,$   
16  $PF_2, PF_n$  simultaneously become the L level. The power-off terminal  
17 POFF of the liquid crystal power source circuit 28 is changed to the L  
18 level. The liquid crystal driving voltages  $V_0 - V_5$  cease to be  
19 generated.

20 The data signal latch clock LP starts reappearing at a time  $t_7$ . In  
21 the same manner as embodiment 1, the output voltage  $INV_{OUT}$  of  
22 the inverter  $INV_2$  becomes the H level at a time  $t_8$ . As discussed  
23 above, the outputs  $PF_1, PF_2, PF_n$  also become the H level at a time  
24  $t_9$  after a 1 - 2 frame period from time  $t_8$ . In consequence of this,  
25 the power-off terminal POFF of liquid crystal power source circuit 28  
26 is changed to the H level. The liquid crystal driving voltages  $V_0 - V_5$   
27 which are in turn applied to the drivers are generated. As explained  
28

1 earlier, the outputs  $T_1, T_2, T_n$  become the H level at a time  $t_{10}$  which  
2 is later by 1-frame period,  $T_F$ , than the time  $t_9$ . The liquid crystal  
3 driving voltages  $V_0-V_5$  are supplied to the scan and signal electrodes  
4 of the liquid crystal display panel 22. Then the liquid crystal  
5 resumes display mode.

6 When the forced display blank control signal DFF on the part of  
7 the liquid crystal display controller 12 becomes the L level at a time  
8  $t_{11}$ , the outputs  $T_1, T_2, T_n$  also become the L level. Correspondingly,  
9 the forced display blank control signal DF on the side of the liquid  
10 display module unit 70 assumes the L level. The liquid crystal  
11 display panel 22 enters a display-off period C. At a time  $t_{12}$  after a  
12 1 - 2 frame period from time  $t_{11}$ , the output Q of the D-type flip-flop  
13 78b of the power on/off control circuit 78<sub>1</sub> is changed to the L level.  
14 The outputs  $PF_1, PF_2, PF_n$  also become the L level. As a result, the  
15 power-off terminal POFF of the liquid crystal power source circuit 28  
16 also assumes the L level. Then the generation of the liquid crystal  
17 driving voltages  $V_0 - V_5$  stops. As described above, the forced  
18 display blank control signal DE on the side of the liquid crystal  
19 display controller 12 becomes the L level, after stopping the liquid  
20 crystal drive, and after a constant period has elapsed, no voltage is  
21 applied to the liquid crystal drivers. Relations in potential with  
22 respect to the logic power source  $V_{CC}$  and the liquid crystal driving  
23 voltages  $V_0 - V_5$  are maintained by the sequence during such a  
24 power-off period. A through current and a parasitic bipolar current  
25 within the driver are restrained, thereby protecting the liquid crystal  
26 display panel and the drivers as well.

1 In accordance with this embodiment, after the clocks have been  
2 supplied to the liquid crystal module, the liquid crystal power source  
3 circuit 28 is powered on. The liquid crystal power source circuit 28  
4 is powered off when stopping the output of the clocks. Rush currents  
5 become dispersive or occur with a time difference by the auto-  
6 sequence of such energizing of the power source. As is similar to the  
7 above, it is feasible to protect the liquid crystal panel constituting the  
8 liquid crystal display module, the drivers, and the liquid crystal  
9 power source circuit as well.

10 Incidentally, in the embodiments discussed above, the signal  
11 management control units are incorporated into the scan drivers LSI.  
12 It is because the number of the I/O signal lines is smaller than that  
13 of the signal drivers LSI, and the display frame region is broad.  
14 Hence, an allowance for the area of the circuit board mounted with  
15 the signal management control units is large. This embodiment has  
16 dealt with the display device based on a simple matrix liquid crystal  
17 panel. The present invention is not limited to this type of display  
18 device but may be applied to an active matrix type liquid crystal  
19 display device. In such a case, it is desirable that the signal  
20 management control units be incorporated into gate drivers LSI. On  
21 this occasion, the gate drivers LSI are controlled so that all the gates  
22 are turned on when stopping the clocks. Source drivers are  
23 controlled to output the same potential on the data side as that on  
24 the common side. All the pixel electric fields are set in a non-  
25 application state. Besides, the present invention is applicable not  
26 only to the displays but also to display devices whose display quality  
27 is deteriorated by the DC drive as can be seen in an electronic device  
28

and a plasma display to which the liquid crystal device is, as in the case of a liquid crystal photo arithmetic device, widely applied.

In the respective embodiments discussed above, the liquid crystal module incorporates a means for detecting an abnormality in the signal supplied from the liquid crystal module controller 12 and a means for eliminating this abnormal state of the signal beforehand or afterwards. The following distributive arrangement may, however, be adoptable. Some of components of those means are provided in the liquid crystal module, while the rest of them are provided in the system (controller). For example, the plurality of signals (SP, LP, FR) which may cause a DC driver of the liquid crystal panel are different from each other in terms of frequencies and pulse duties. Therefore, those signals are converted into a single composite signal by use of a non-coincidence gate (Exclusive OR gate). The composite signal is sent back to the system, and the abnormal state is checked by a judgment circuit. The abnormal state is eliminated by an output thereof. An additional arrangement is that the indicator display is effected by using a display body other than that on the side of the LCD module. The following is another adoptable method. The output of the terminal  $T_n$  of the scan driver  $46_n$  in the embodiment of FIG. 1 is returned to the system, and the logic and liquid crystal system power sources are on/off-controlled by fixed procedures (sequence).

Another cause for deteriorating the liquid crystal panel will be elucidated. The deterioration may be caused by the fact that the liquid crystal panel is driven by the effective DC components due to a decay in the output of a specific driver. Deterioration may also be caused by value shifts of the liquid crystal driving voltages  $V_0 - V_5$

1 which are derived from an abnormality in the voltage dividing  
2 circuit 28e of the liquid crystal power source circuit 28 shown in FIG.

3 7. Those abnormal conditions are detectable as fluctuations in the  
4 power source current and voltage and, therefore, eliminated by the  
5 above-described abnormality eliminating means.

6 Industrial Applicability:

7 As discussed above, in a flat display device according to the  
8 present invention, when stopping the oscillations of signals  
9 transferred from the display control unit, the DC drive of the liquid  
10 crystal is forcibly stopped by the signal management control means  
11 of the display body module. It is, therefore, possible to prevent  
12 deterioration in the display body which is derived from the DC drive.  
13 Besides, power source rush currents can be reduced. The present  
14 invention is applicable not only to the liquid crystal display device  
15 but also to a plasma display device and the like. The present  
16 invention is suitable for use with such display devices that the  
17 display quality and life-span of the display body are unrestorable  
18 due to the abnormality in the driving signals.  
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